Amendments to the Claims:

This listing of claims replaces all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently amended) A processor, ~~comprises~~ comprising:

an execution unit for executing multiple context threads, said execution unit comprises:

an arithmetic logic unit to process operands for executing threads;

a multiplexor;

control logic to control the operation of the arithmetic logic unit and the multiplexor;

an immediate data bus coupled from the output of the control logic to an input of the multiplexor to provide immediate data to the arithmetic logic unit through the multiplexor;

a general purpose register set that includes a plurality of general purpose registers coupled to the input of the multiplexor to provide register operand data to the arithmetic logic unit through the multiplexor; and

a read transfer register coupled to the input of the multiplexor to provide operand data from a memory device;

wherein execution of a register instruction causes data from one or more input sources connected to the multiplexor to be transferred through the multiplexor into the arithmetic logic unit and causes data to be transferred through the arithmetic logic unit to one of the general purpose registers.

2. (Currently amended) The processor ~~execution unit~~ of claim 1 wherein the register instruction includes a bit mask specifying which one or more bytes of the data are affected and causing the bytes of the data specified by the bit mask to be loaded into the arithmetic logic unit from the immediate data bus and the bytes of the data not specified to be loaded from the read transfer register.

3. (Currently amended) The processor ~~execution unit~~ of claim 1 wherein the register instruction includes a bit mask specifying which one or more bytes of the data are affected and causing the bytes of the data specified by the bit mask to be loaded into the arithmetic logic unit from the immediate data bus and the bytes of the data not specified to be loaded from the general purpose register.

4. (Currently amended) The processor ~~execution unit~~ of claim 1 further comprising:

a bypass bus coupled from the output of the arithmetic logic unit to an input of the multiplexor; and

control logic to control the execution of a series of pipelined instructions wherein each pipelined instruction may specify a read part and a write part, where the read part of one pipelined instruction specifies a read address that is the same as a write address of the write part of another pipelined instruction causing the data being written by the write part to be available to the read part in the same processor cycle.

5. (Currently amended) A method for executing multiple context threads ~~comprises~~ comprising:

processing operands for an executing context thread of multiple context threads through a multiplexor and an arithmetic logic unit;

operating control logic connected to the arithmetic logic unit and the multiplexor;

providing immediate data on an immediate data bus coupled from the output of the control logic to an input of the multiplexor;

providing operand data to the arithmetic logic unit from a general purpose register coupled to the input of the multiplexor;

providing operand data from a memory device through a read transfer register coupled to the input of the multiplexor; and

executing a register instruction to cause data from one or more input sources connected to the multiplexor to be transferred through the multiplexor into the arithmetic logic unit and to cause data to be transferred through the arithmetic logic unit to one of the registers.

6. (Original) The method of claim 5 wherein executing a register instruction further comprises:

including a bit mask; and

causing the bytes specified by the bit mask to be transferred through the multiplexor from the immediate data bus and the bytes not specified to be transferred through the multiplexor from the transfer register.

7. (Original) The method of claim 5 wherein executing a register instruction further comprises:

including a bit mask; and

causing the bytes specified by the bit mask to be transferred through the multiplexor from the immediate data bus and the bytes not specified to be transferred through the multiplexor from the general purpose register.

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9. (New) A processor comprising:

a plurality of microengines, each of the microengines comprising:

a control store, the control store storing a microprogarm loadable by a core processor;

controller logic including an instruction decoder and program counter units maintained in hardware;

context event switching logic, the context event switching logic receiving messages and arbitrating for threads;

an execution box data path including an arithmetic logic unit (ALU), general purpose registers and multiplexors providing input to the ALU;

a write transfer register stack; and

a read transfer register stack.

10. (New) The processor of claim 9 in which the plurality of general purpose registers comprises:

a first bank of general purpose registers; and

a second bank of general purpose registers.

11. (New) The processor of claim 10 in which the first bank general purpose registers and the second bank general purpose registers are windowed.

12. (New) The processor of claim 9 in which registers contained in the write transfer register stack and registers contained in the read transfer register track are windowed.

13. (New) The processor of claim 9 in which the write transfer register stack stores write data to a resource.

14. (New) The processor of claim 9 in which the read transfer register stack stores return data from a shared resource.

15. (New) The processor of claim 9 in which the execution box data path maintains a five-stage micro-pipeline.

16. (New) The processor of claim 15 in which the five-stage micro-pipeline comprises:

lookup of micro-instruction words;

formation of general purpose register file addresses;

read of operands from the general purpose registers;

ALU shift or compare operations; and

write-back of results to the general purpose registers.